Lab 4

Michael Lankford

Station #11 Partner: Vladislava Sicicorez

Prelab:

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Diagram

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Purpose:

The purpose of lab 4 was to become more acquainted with Xilinx Vivado by implementing a circuit that had 3 inputs and gave an output that was equal to the square of the input.

Lab Procedure:

We started the lab by opening Vivado and creating an RTL project that was set to ‘VHDL’ target language. We continued by creating a design source file called Lab\_4 with I/O ports for the file. The inputs were a, b, and c and the outputs were u, v, w, x, y, and z. We then wrote 6 lines of code that would simulate the boolean expressions for u, v, w, x, y, and z from the prelab.

Next, we created a simulation file titled square, copy and pasted the I/O from Lab\_4 into square, created std\_logic signals for the inputs and outputs, and also added a port map to Lab\_4. Finally, we added our 8 test cases from the prelab into the program(000, 001, 010, 011, 100, 101, 110, 111).

We then ran the Behavioral Simulation and took note of the waveform output, created one final program that would allow us to enter our inputs on a Basys 3 board, then ran Synthesis, Implementation, and finally Generated Bitstream. We then connected the Basys 3 board to the computer and manually tested the outputs on it.

Vivado Code-

Graphical user interface, text, application, email

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Basys 3 Board-

Input: 000

A picture containing electronics

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Input: 001

A picture containing text, electronics

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Input: 010

A picture containing electronics

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Input: 011

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Input: 100

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Input: 101

A picture containing text, electronics, circuit

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Input: 110

A picture containing electronics, indoor

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Input: 111

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Bitstream-

Chart

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Conclusion:

In this lab, we further acquainted ourselves with the Xilinx Vivado software by making a circuit that took 3 inputs and produced outputs that were equal to the square of the input. The results of this lab supported our truth table from the prelab, showing that for the input 000 there was an output 000000, for input 001 there was output 000001, for input 010 there was output 000100, for input 011 there was output 001001, for input 100 there was output 010000, for input 101 there was output 011001, for input 110 there was output 100100, and for input 111 there was output 110001. We were able to manually test these with the Basys 3 board which had switches we could move between high and low input.

Finally, I believe physically constructing a circuit is more beneficial to my learning.

Observations:

The main observation I have to improve my performance on future experiments would be to remember every step for the setup of the programs. For this experiment, I ended up forgetting to set the family to artix-7 which showed gave us an error when we tried to generate bitstream.